FREE STARTER CHAPTER

Break Into Chip Design

Your first chip lab: digital + analog in one evening

4 real lab runs with outputs · how a chip is born · the 4 career tracks
India salaries and employers · what recruiters check · a 90-day snapshot
a 6-question quiz · and a ₹499 pre-launch offer for the full book

Part of the 90-Day Semiconductor Career Launchpad for ECE / EEE
students and early-career engineers

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WHY THIS, WHY NOW

Chip design is hiring — and India is building the bench

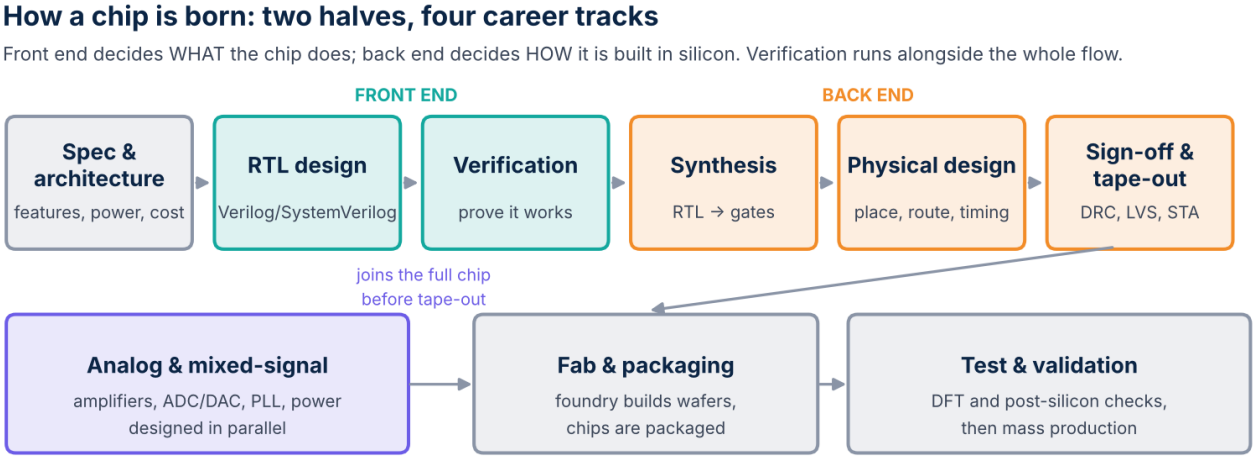
Every phone, EV, data-centre server and smart meter runs on chips, and the people who design them are in short supply worldwide. India has set a target of training **85,000 semiconductor design engineers** under its Chips to Startups programme. The US industry alone may face a shortfall of about **67,000** technicians, engineers and computer scientists by 2030. Malaysia plans 60,000 new skilled workers and Vietnam 50,000 chip engineers by 2030.

The gap is not talent — it is **direction**. Most ECE/EEE students know some Verilog and some circuits, but cannot answer three questions: *Which role fits me? What exactly do recruiters check? What can I build in the next 90 days to prove it?* This chapter answers all three, and you will run four real labs — two digital, two analog — to see the work for yourself.

Where demand is heading (next 5 years)

AI accelerators — every AI model runs on custom silicon; verification and physical-design teams grow fastest.
Automotive and EV electronics — battery management, motor control and radar chips need analog and mixed-signal skills.
Chiplets and advanced packaging — chips built from smaller dies; new roles in integration, test and signal integrity.
Power and edge IoT — billions of low-power devices; strong demand for low-power design and analog front ends.
These are directional trends, not forecasts with numbers; the full book tracks job postings to show which skills each trend is pulling.

How a chip is born



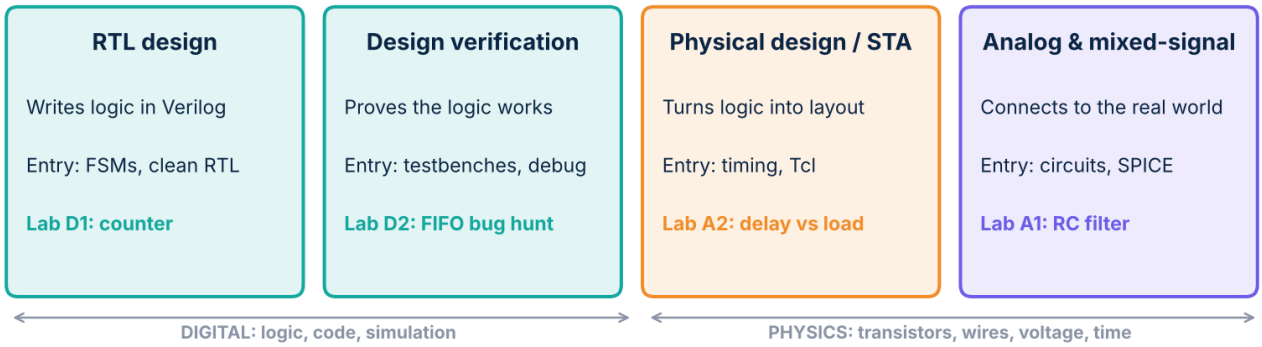
Read the flow left to right: a spec becomes Verilog (RTL), verification proves it, synthesis turns it into gates, physical design turns gates into geometry, and sign-off checks it before the design is sent to the foundry (tape-out). Analog blocks are designed in parallel and join the full chip before tape-out. Each box is a team — and a job title.

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THE FOUR TRACKS

Digital or analog? Choose by skill, not salary

Digital and analog: where each track sits, and how the labs in this chapter map to them



Track	What you do all day	Fresher pay in India*	Best first step
RTL design	Write Verilog for blocks: FSMs, FIFOs, bus interfaces	₹6–8 LPA	Lab D1, then a UART
Design verification	Build testbenches, hunt bugs, measure coverage — the largest hiring track	Tracks RTL design pay	Lab D2, then SystemVerilog classes
Physical design / STA	Floorplan, place, route, close timing with Tcl scripts	₹6–12 LPA	Lab A2, then an open RTL-to-layout flow
Analog & mixed-signal	Design amplifiers, ADCs, PLLs, power circuits in SPICE	Premium over generalist digital roles	Lab A1, then a current mirror

*Source: Futurense, Chip design engineer salary in India (2026). Top MNC offers are higher (for example Intel ₹18–24 LPA, NVIDIA ₹22–28 LPA including stock). Training-linked routes start at ₹3.5–8 LPA. Pay varies by city, company and skills; treat these as ranges, not promises.

Who is hiring in India

Intel, NVIDIA, Qualcomm, Texas Instruments, Samsung, AMD, TSMC and Saankhya Labs are among the employers named in recent salary surveys, alongside design-service companies that hire freshers in volume. Service companies teach breadth fast; product companies go deep on one chip. Both are good first jobs.

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LAB D1 · DIGITAL · RTL DESIGN

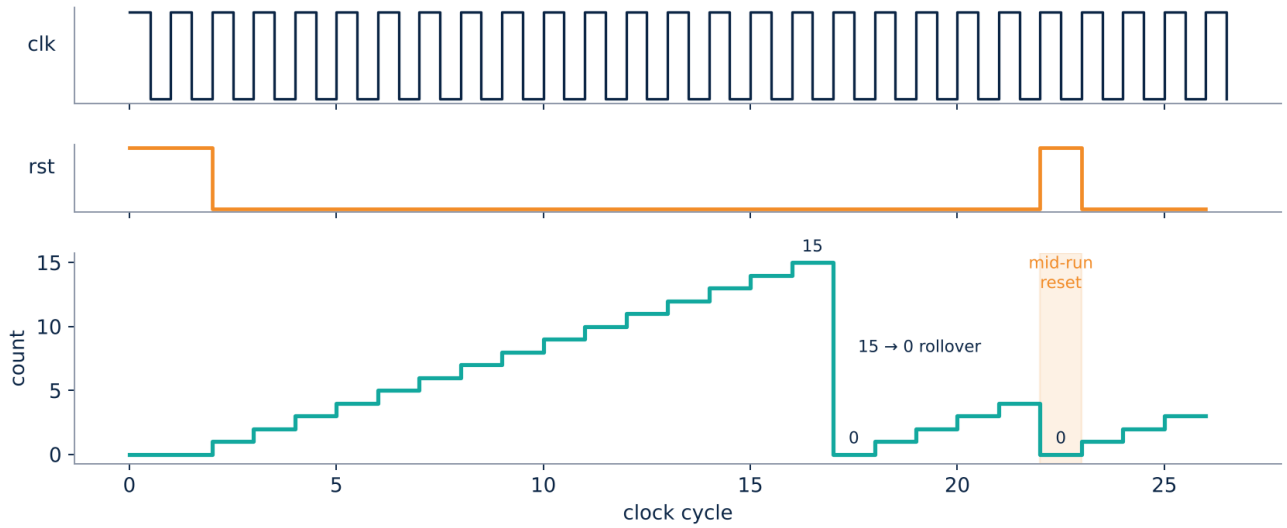
A 4-bit counter — and the test that proves it

The problem. A system must count clock edges from 0 to 15, then wrap to 0, and must restart cleanly whenever reset is pressed — even in the middle of a count. Four bits hold 16 states. The value updates only on the rising edge of the clock.

```
module counter4 (
    input  wire       clk,
    input  wire       rst,
    output reg  [3:0] count
);
  always @(posedge clk) begin
    if (rst)  count <= 4'd0;          // synchronous reset
    else      count <= count + 1'b1;  // 15 + 1 wraps to 0 in 4 bits
  end
endmodule
```

The testbench drives a 100 MHz clock, holds reset for 2 cycles, counts for 20 cycles (so it must roll over), fires a reset mid-run, and compares the design against a reference model after every edge. This is the actual output from Icarus Verilog:

Lab D1 · 4-bit counter: reset, count, rollover (Icarus Verilog run)




```
RESULT: PASS - reset and rollover verified (25 checks)
```

What this proves to a recruiter

You can write synthesisable sequential logic, you understand why non-blocking **<=** is used for flip-flops, and you test edge cases (rollover, mid-run reset) instead of only the happy path. Put the code, the testbench and this waveform on GitHub with a 5-line README.

Interview follow-up you should expect: "What changes if the reset is asynchronous?" (Answer: add *posedge rst* to the sensitivity list; the counter clears immediately instead of at the next clock edge.)

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LAB D2 · DIGITAL · DESIGN VERIFICATION

Find the hidden FIFO bug

The problem. A 4-entry FIFO (first-in, first-out buffer) passes every normal test. But one line is wrong. A verification engineer's job is to find it *before* it reaches silicon, where a fix costs months. Here is the buggy write logic:

```
// BUG: a write is accepted even when the FIFO is full
if (wr_en) begin
  mem[wptr] <= din;
  wptr      <= wptr + 1'b1;
end
```

The testbench writes **five** values into a **four**-deep FIFO — one too many — then reads four back and compares each one with a reference queue model. Same testbench, two designs, real output:

Lab D2 · the same self-checking testbench run on both designs

Buggy FIFO — data 10 is lost

```
WRITE 10  (full=0 before write)
WRITE 20  (full=0 before write)
WRITE 30  (full=0 before write)
WRITE 40  (full=0 before write)
WRITE 50  (full=1 before write)
READ  50  expected 10  <-- MISMATCH
READ  20  expected 20  ok
READ  30  expected 30  ok
READ  40  expected 40  ok
RESULT: FAIL - 1 mismatches at the full boundary
```

Fixed FIFO — write blocked when full

```
WRITE 10  (full=0 before write)
WRITE 20  (full=0 before write)
WRITE 30  (full=0 before write)
WRITE 40  (full=0 before write)
WRITE 50  (full=1 before write)
READ  10  expected 10  ok
READ  20  expected 20  ok
READ  30  expected 30  ok
READ  40  expected 40  ok
RESULT: PASS - full-boundary test passed
```

What happened. The fifth write (50) was accepted while the FIFO was full, the write pointer wrapped around, and 50 overwrote the oldest value, 10. The fix is one condition: `if (wr_en && !full)`. Without a boundary test, this bug would pass every normal test you could write.

Real-world application

FIFOs sit between every two blocks that run at different speeds: camera sensor to image processor, network port to memory, CPU to display. An overflow bug silently drops data — a frozen video frame, a corrupted packet. This is why verification is the largest hiring track.

Interview question: "A FIFO passes normal tests but fails when full. How do you investigate?" Reproduce the boundary, inspect occupancy and pointer updates, compare against a reference model, check overflow handling.

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LAB A1 · ANALOG · CIRCUITS

An RC low-pass filter: theory meets simulation

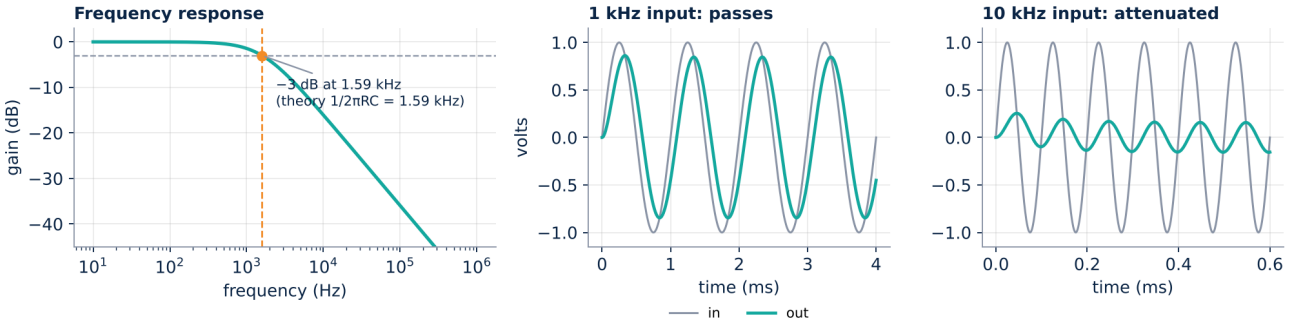
The problem. A sensor signal carries high-frequency noise. A resistor and a capacitor make the simplest filter: low frequencies pass, high frequencies are reduced. The cutoff (where the output falls to about 70.7% of the input, or −3 dB) is:

$$f_c = 1 / (2\pi R C) = 1 / (2\pi \times 1\ k\Omega \times 100\ nF) \approx 1.59\ kHz$$

```
* ngspice netlist
V1 in 0 DC 0 AC 1
R1 in out 1k
C1 out 0 100n
.ac dec 50 10 1meg
.meas ac fc WHEN db(v(out)) = -3.0103

Result from the run:   fc = 1.591551e+03  (1,591.6 Hz; theory 1,591.5 Hz)
```

Lab A1 · RC low-pass filter, R = 1 kΩ, C = 100 nF (ngspice run)



The 1 kHz signal comes through nearly intact; the 10 kHz signal is cut to about a sixth of its size. Above the cutoff, the output falls by 20 dB for every tenfold rise in frequency — the straight slope on the left plot.

Where this shows up in real chips

Every analog-to-digital converter needs an **anti-aliasing filter** in front of it; touchscreens, microphones and ECG front ends filter noise exactly like this. And in digital chips, every wire is a tiny R and C — which is why signals take time to travel (see Lab A2).

Interview question: "If C doubles, what happens to the cutoff?" It halves, because f_c is inversely proportional to C.

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LAB A2 · ANALOG MEETS DIGITAL · PHYSICAL DESIGN

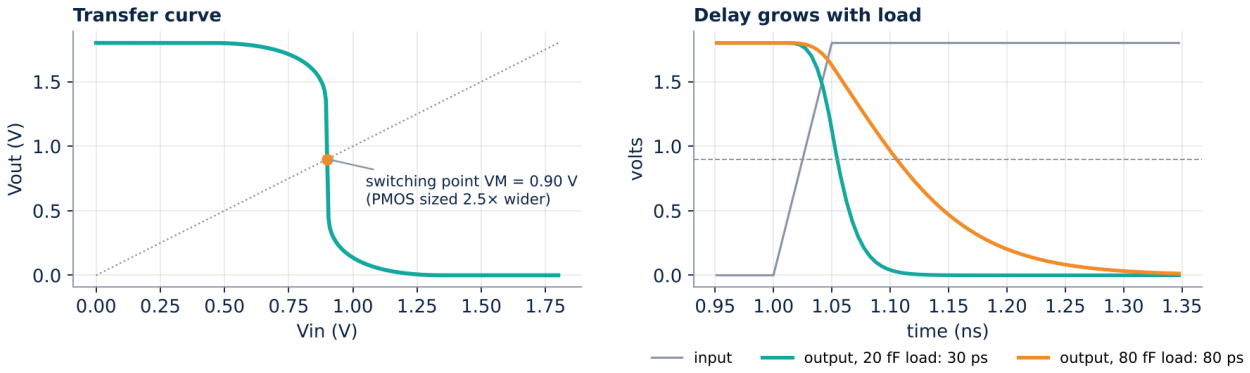
Inside a logic gate: the CMOS inverter

The problem. Every digital gate is really an analog circuit: a PMOS transistor pulls the output up, an NMOS pulls it down. Two questions decide whether a chip works and how fast it runs: *at what input voltage does the gate switch?* and *how long does the output take to change?*

```
* CMOS inverter, VDD = 1.8 V (teaching models, not a foundry PDK)
MP out in vdd vdd pmos_t W=2.5u L=0.18u
MN out in 0   0   nmos_t W=1u   L=0.18u
CL out 0 20f            * load: the wires and gates this output drives

Results from the run:
  switching point  vm    = 0.900 V
  delay, 20 fF     tphl  = 29.6 ps
  delay, 80 fF     tphl  = 80.5 ps
```

Lab A2 · CMOS inverter at 1.8 V (ngspice, teaching models)



The PMOS is sized 2.5× wider because holes move more slowly than electrons; that balances the gate so it switches at exactly half the supply (0.90 V). Quadrupling the load capacitance made the gate about 2.7× slower.

Why this matters for your career

This is the bridge between the two worlds. **Physical design and timing engineers** spend their days on exactly this effect: long wires and big fan-outs add capacitance, gates slow down, and a path misses its clock. **Analog engineers** size transistors like this for every circuit. Understanding one inverter deeply is worth more in an interview than memorising ten definitions.

Interview question: "Why is the PMOS usually made wider than the NMOS?" Lower carrier mobility in PMOS; widening it balances rise and fall times.

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THE COMPANY'S VIEW

What a real hiring team asks for

An NVIDIA posting for ASIC Verification Engineer (New College Grad 2026) asked for: a BS/MS in electrical or computer engineering; exposure to ASIC design, verification and computer architecture; strong programming and debugging in SystemVerilog, C/C++ or Python/Perl; object-oriented programming; and communication. *Preferred:* test plans, constrained-random and coverage-driven verification, UVM, assertions, and experience with AI coding tools.

What they ask	Evidence you can build	Where in this book
Verilog / SystemVerilog	Counter and FIFO with clean RTL	Lab D1, Ch 7
Testbench development	Self-checking tests with boundary cases	Lab D2, Ch 8
Debugging	A documented bug, reproduction and fix	Lab D2, Ch 16
Scripting	A Python script that runs your regressions	Ch 14
Communication	A README and a 3-minute project walkthrough	Ch 16, Ch 18

Your 90-day snapshot

Phase	Days	Focus	Checkpoint
1 · Foundations	1–21	Logic, CMOS, timing, Verilog basics	50 HDLBits problems + an FSM project
2 · Track deep dive	22–49	DV, physical design or analog; Linux, Python, Tcl	One track lab done + one script
3 · Portfolio	50–77	Two projects, tested and written up	2 projects on GitHub with READMEs
4 · Get hired	78–90	CV, LinkedIn, outreach, interview sprint	CV live, 20 applications, 1 mock interview

After day 90 — the next phase of skilling: UVM and formal verification for DV; static timing and low-power design for PD; data converters and PLLs for analog; and a real tape-out of a tiny design on a shared shuttle such as Tiny Tapeout. The full book maps each of these to the role it unlocks.

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QUICK QUIZ · 6 QUESTIONS · 3 MINUTES

Test yourself

Score 5 or more and you are ready for Phase 1. Answers are at the bottom of this page — no peeking.

1. A 4-bit counter is at 15. What is its value after the next clock edge (no reset)?

a) 16 b) 0 c) 15 d) undefined

2. In the buggy FIFO, which value was lost?

a) the newest (50) b) the oldest (10) c) none d) all of them

3. R = 2 kΩ, C = 100 nF. The cutoff frequency is about:

a) 3.2 kHz b) 1.59 kHz c) 796 Hz d) 159 Hz

4. The inverter's load capacitance goes up. Its delay:

a) goes down b) stays the same c) goes up d) becomes zero

5. Which track spends most of its time writing testbenches?

a) RTL design b) design verification c) physical design d) analog

6. Tape-out means:

a) the chip is shipped to customers b) the final design is sent to the foundry c) the RTL is written d) the chip fails test

Answers: 1-b · 2-b · 3-c · 4-c · 5-b · 6-b

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Sources: India Semiconductor Mission / Chips to Startups (85,000 target); SIA–Oxford Economics (US shortfall of 67,000 by 2030); Stanton Chase (Malaysia and Vietnam targets); Futurense (India salaries, 2026); NVIDIA careers posting (New College Grad 2026). All lab results produced with Icarus Verilog and ngspice; source files are included in the lab pack.